

REMARKS

Entry of the above amendment and reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1, 2, 6-10, 15-16 are pending in this case. Claims 15 and 16 are added herein to more completely cover that which Applicant regards as the invention.

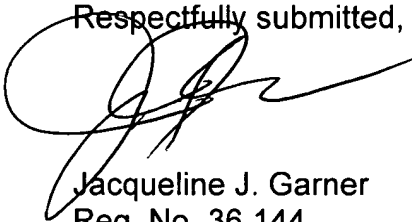
The Examiner rejected claims 1, 2 and 6 to 10 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Applicant respectfully submits that the specification provides support for partial extension of the via as claimed in claims 1 and 10. The teaching of a partial via etch is provided at page 6 lines 1-4 and is illustrated in FIG. 2C. The partial via is further discussed on page 7 lines 26 through page 8 line 4. Here the second embodiment is discussed beginning after the partial via etch of FIG. 2C. Instead of continuing with the full via etch as in the first embodiment, "[a]fter half the via 116 is etched (e.g., through the IMD 110), the BARC layer 120 is deposited and the trench pattern is formed as shown in FIG. 3A." Etching of half the via is further discussed with respect to the third embodiment at page 8 lines 15-24. FIGs. 2C, 3A, and 4A all illustrate a partial via etch.

Applicant respectfully submits that the specification provides support for "but not etching said interlevel dielectric layer" as recited in claim 10. FIGs. 2C, 3A, and 4A all illustrate a partial via etch where the IMD 110 is etched but the ILD 106 is not. As discussed on page 6, lines 1-14, it is not until after the partial via etch that the shelf layer 116 is opened and the via is finally etched through ILD 106. As the shelf layer overlies the ILD 106, it is clear to those of ordinary skill in the art from the text and corresponding FIGs 2C and 2D that the ILD 106 is not etched during the partial via etch. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1, 2, 6-10, 15, and 16. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'J. Garner', written over the typed name.

Jacqueline J. Garner
Reg. No. 36,144

Texas Instruments Incorporated
P. O. Box 655474, M.S. 3999
Dallas, Texas 75265
Phone: (214) 532-9348
Fax: (972) 917-4418